In the Specification:

In the Description of the Invention

Referring to the prior amendment filed 24 August 2004, please replace the single paragraph of text beginning on page 5, line 23 to page 6, line 12 in the Office Action reply with the text below. The replacement text below includes the Examiner's recommendation to amend "55" to "58" on page 6, line 12 and also includes an amendment to properly identify the low voltage logic gate and high voltage logic gate consistent with the other specification text, Figures 2A-C, and 3A-B. Added matter is shown by underline (underline) and deleted matter is shown by strikethrough (~~strikethrough~~). No new matter has been added.

Next, as shown in Figures 3A and B at step (iv), a high voltage (HV) gate oxide layer 68, for example having an approximate 250 Å thickness, is formed over the substrate 46. The oxide layer 68 is masked with a patterned photoresist. The exposed part of the oxide layer 68 is then etched to reveal portions of the underlying substrate 46 as shown in step (v). Next, in exposed areas 52, 54, a second or subsequent, thinner oxide layer will be formed. The formation of the first or second oxide layer may be carried out by thermal oxidation of the substrate, chemical vapor deposition, or atomic layer deposition. As shown in step (vi), a first device area will be used to form an EEPROM tunnel oxide layer 58, a second device area will be used to form a ~~high~~ low voltage logic gate oxide layer 56, and a third device area will be used to form a ~~low~~ high voltage logic gate oxide layer 67. Referring to Figure 2B, an N+ region may be developed in the EEPROM cell area to form a control gate 80. The ~~HV~~ LV gate oxide layer 56 and the tunnel oxide layer 58

each, for example, approximately 70 Å thick, have been formed on the exposed portions 52, 54 of the substrate 46. This layer of thin gate oxide 56, 58 serves as a gate oxide 56 for the low voltage (LV) logic gate and a tunnel oxide 58 for the EEPROM cell respectively. The low voltage logic gate oxide layer 56 may have essentially the same thickness as the tunnel oxide layer ~~55~~ 58.